IMPLEMENTATION AND VERIFICATION OF FILTER USING APPROXIMATE MULTIPLIER

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ABSTARCT

With the rapid advancements in digital technology, there is a growing demand for devices that offer high performance, fast response, and compact size, particularly for applications like image processing. However, the arithmetic operations involved in adders and multipliers often lead to increased logic size in VLSI implementations, resulting in significant area and power consumption when using traditional designs. To address this, the paper proposes an implementation of a 16×16 multiplier using modified 5:2 compressors, where conventional summing units and repeated adders are replaced with XORMUX adders. This approach effectively reduces both area and power requirements compared to standard adders and multipliers. Approximate multipliers, as used here, deliver results close to those of exact multipliers, making them highly efficient in terms of accuracy, power, and area, offering a superior alternative to exact designs.

INTRODUCTION

In today's digital age, numerous devices with a wide range of applications, such as image and video processing, are commonplace. However, these devices often face challenges due to a low signal-to-noise ratio (SNR), leading to signal interference that hampers computations like addition and multiplication, which are fundamental operations in many digital systems. Since multiplication and division are essentially based on repetitive addition and subtraction, it is critical that these operations be performed with minimal noise and interference. This paper focuses on improving arithmetic operations, specifically through the use of approximate multipliers. The proposed architecture incorporates filter banks, which consist of filters that decompose coefficients, and modifies traditional adders and multipliers using XOR-MUX adders and approximate multipliers. By using XOR-MUX full adders instead of regular full adders, the approach reduces the logic gate count needed for the approximate multiplier, while also minimizing the area occupied by FIR filters.

LITERATURE SURVEY

1. **FPGA Implementation of XOR-MUX Full Adder-Based DWT for Signal Processing Applications:**

Recent advancements in digital technology, particularly in signal processing and image processing, demand high-performance devices that are fast, compact, energy-efficient, and low-latency. These devices are critical in applications such as signal processing, audio processing, and software-defined

radio. However, traditional digital systems often face challenges with high logic complexity, power consumption, and large area requirements in VLSI implementations, primarily due to the arithmetic operations involved in adders and multipliers. The Digital Wavelet Transform (DWT) architecture, which relies heavily on filter banks containing multiple adders and multipliers for coefficient decompositions, exacerbates these issues, leading to increased logic size and power consumption. To address these challenges, this work introduces a novel DWT approach by replacing conventional adders and multipliers with XOR-MUX adders and truncated multipliers. This reduces the logic size from 2n to n, thereby enhancing efficiency. The proposed DWT architecture, designed using VHDL, is implemented on the FPGA XC6SLX9-2TQG144, demonstrating significant improvements in delay, area, and power consumption.

2. **A Low Power Signed Redundant Binary Vedic Multiplier:**

This study presents a high-speed signed Vedic multiplier (SVM) architecture based on redundant binary (RB) representation and the Urdhva Tiryagbhyam (UT) sutra, marking the first extension of Vedic algorithms to signed numbers. The proposed architecture addresses the carry propagation problem inherent in UT sutra by leveraging carry-free addition made possible by RB representation. This innovation not only resolves the carry issues but also enhances performance in terms of speed. The design is implemented in VHDL and synthesized using Xilinx ISE 14.4 across various FPGA devices. Compared to conventional and other Vedic multiplier architectures, the proposed signed Vedic multiplier offers superior speed and performance, making it a promising solution for high-speed and low-power applications.

EXISTING METHOD

The implementation and verification of filters using approximate multipliers involve incorporating low-precision multipliers into filter designs to reduce power consumption, area, and delay while maintaining acceptable output accuracy. Existing methods typically rely on approximate arithmetic techniques, such as truncated or reduced-precision multipliers, which replace exact multipliers with simplified versions that reduce computational complexity. These approximate multipliers are used in digital filters (such as FIR or IIR filters) to achieve energy-efficient solutions for applications like image processing, signal processing, and communication systems. Verification of these filters involves comparing the performance of the approximate filters with traditional, high-precision filters in terms of output accuracy, speed, power consumption, and area. Several simulation tools are used to assess the impact of approximation errors, ensuring that the trade-off between efficiency and accuracy meets the system's requirements.

PROPOSED METHOD

The 16-bit Ladner-Fischer adder is an efficient parallel adder structure that minimizes logic depth but comes with a large fan-out requirement, which can extend up to n/2. In 1980, Fischer and

Richard Ladner introduced a parallel algorithm for efficiently computing prefix sums. This approach constructs a circuit where each node performs an addition between two numbers. Their design allows for a trade-off between the depth of the circuit and the number of nodes, providing flexibility in balancing speed and resource usage.

The 16-bit Han-Carlson adder combines elements from both the Kogge-Stone and Brent-Kung adder designs. While it reduces the number of cells and wire tracks compared to the Kogge-Stone adder, it sacrifices one additional logic level. The design works by transmitting generate and propagate signals from odd bits down the prefix tree, where they eventually recombine with the even bits' carry signals to produce the final carry bits. This hybrid structure achieves reduced complexity, though at the expense of adding an extra stage to the carry-merge path, thus increasing the total logic depth.

APPLICATIONS

1. **Digital Signal Processing (DSP)** – Essential for tasks like audio processing, speech recognition, and image enhancement by manipulating signals for clearer output.
2. **Wireless Communication** – Vital in filtering out unwanted noise in communication technologies such as 5G, Wi-Fi, and Bluetooth for enhanced signal quality.
3. **Biomedical Signal Processing** – Used to clean bio-signals like ECG and EEG by removing noise, ensuring more accurate readings.
4. **Radar and Sonar Systems** – Improves detection precision by filtering out irrelevant frequency components, enhancing system performance.
5. **Embedded and IoT Systems** – Crucial in low-power devices like smart wearables and IoT sensors for efficient data processing and signal handling.
6. **Artificial Intelligence and Machine Learning** – Employed in preprocessing raw data to remove noise before inputting it into neural networks for more accurate learning and predictions.
7. **High-Speed Computing Systems** – Boosts performance in FPGA and ASIC-based hardware accelerators by optimizing data processing speeds.

ADVANTAGES

1. **Reduced Power Consumption** – XOR-MUX Full Adder and Approximate Multipliers offer lower power consumption compared to conventional designs.
2. **Faster Computation** – Fewer logic gates are used, leading to quicker processing and reduced delay.
3. **Optimized Hardware Efficiency** – Uses fewer transistors, making it a cost-effective solution for VLSI designs.
4. **Enhanced Energy Efficiency** – Ideal for battery-operated and portable devices due to minimized power usage.
5. **Fault Resilience** – Approximate computing tolerates minor errors while preserving acceptable performance levels.
6. **Scalability** – Can be adapted to a wide range of digital systems, including FPGAs, ASICs, and microprocessors.

DISADVANTAGES

1. **Accuracy Trade-Off** – Approximate multipliers can introduce slight inaccuracies, making them unsuitable for applications where precision is critical.
2. **Design Optimization Challenges** – Achieving the right balance between performance, power consumption, and accuracy requires careful design decisions.
3. **Restricted Use Cases** – They are not ideal for applications demanding high precision, such as medical imaging or scientific computing.
4. **Hardware Complexity** – Despite optimization, the initial design and testing process demands significant expertise.
5. **Error Propagation** – Small errors in approximation-based operations can accumulate over time, potentially affecting the overall system output.

FUTURE SCOPE

AI-based optimization leverages machine learning to dynamically adjust approximation levels according to application requirements, improving computational efficiency. In hardware-aware deep learning, AI accelerators are utilized to enhance inference performance. Quantum computing integration explores quantum-inspired techniques for advanced signal processing through approximate computing methods. Edge computing applications focus on deploying low-power FIR filters in real-time AI/ML edge devices for efficient processing. Adaptive approximate computing develops dynamic strategies to minimize errors and maximize efficiency. Lastly, neuromorphic computing integrates approximate FIR filters into brain-inspired architectures, enabling real-time signal processing in computationally efficient ways.

CONCLUSION

The FIR filter based on XOR-MUX Full Adder and Approximate Multiplier offers a high-speed, low-power alternative to traditional FIR filters, making it well-suited for real-time processing in applications where moderate accuracy is acceptable. This design notably reduces both power consumption and area, which is beneficial for embedded systems, IoT, and DSP applications. However, the trade-off in accuracy means it may not be suitable for applications that require highly precise calculations.

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